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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/649,578	08/26/2003	Masahiro Kimura	59801 (47793)	5969

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EXAMINER	
FRANKLIN, RICHARD B	
ART UNIT	**PAPER NUMBER**
2181	

DATE MAILED: 02/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/649,578	KIMURA ET AL.	
	Examiner	Art Unit	
	Richard Franklin	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☒ Claim(s) *7-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/09/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 13 have been examined.

Drawings

2. Figure 15 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Applicant is advised that should claim 7 be found allowable, claim 8 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k). Claim 7 further limits the receiving buffer with a number of elements while claim 8 limits the interface unit with the same elements. The receiving

buffer and interface unit could be in the same unit and are therefore not distinct elements in the claims.

4. Claim 13 is objected to under 37 CFR 1.75(c) as being in improper form because a multiple dependent claim cannot depend from any other multiple dependent claim. See MPEP § 608.01(n). Accordingly, the claim has not been further treated on the merits.

Claim 13 depends on claim 9, which is dependent on claims 7 and 8. The Examiner has interpreted claim 9 as only depending on claim 7 to examine claim 13, since claim 8 is a duplicate of claim 7 as noted in the objection above.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 5 – 12 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 3 – 6, 8 10 – 16, 18, and 20 of copending Application No. 10/649,231. Although the conflicting claims are not identical, they are not patentably distinct from each other because the application No. '231 discloses all the limitations of the current application except the system memory. However, it would have been obvious to one of ordinary skill in the art to recognize that "a local memory" of application '231 is equivalent to and has the same function to "a system memory" of the current application.

Claim 5 of the current application is read on by claims 4 and 14 of copending Application No. '231. Claim 6 of the current application is read on by claims 5 and 15 of copending Application No. '231. Claims 7 and 8 of the current application are read on by claims 1, 10, 12, and 20 of copending Application No. '231. Claim 9 of the current application is read on by claim 13 of copending Application No. '231. Claim 10 of the current application is read on by claims 3, 11, and 20 of copending Application No. '231. Claim 11 of the current application is read on by claims 6 and 16 of copending Application No. '231. Claim 12 of the current application is read on by claims 8 and 18 of copending Application No. '231.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 11 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 11 recites the limitation "said first, second and third dedicated buses" in Lines 3 and 4 of the claim. There is insufficient antecedent basis for this limitation in the claim.

The Examiner has interpreted this limitation as being removed from the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1, and 12 – 13 are rejected under 35 U.S.C. 102(e) as being anticipated by Lapstun et al. US Patent No. 6,687,022 (hereinafter Lapstun).

As per claim 1, Lapstun teaches a data transferring apparatus comprising: a system bus (Figure 17 Item 145); a system memory coupled to the system bus in order to be able to transfer data to the system bus (Figure 17 Item 82); a decode unit comprising a decode circuit coupled to the system bus in order to be able to transfer

data to the system bus, wherein the decode circuit can perform hardware development on liquid ejection data compressed to be capable of line development (Figure 19, Col 28 Line 19 – Col 33 Line 41); and a data transferring unit for transferring the liquid ejection data compressed to be capable of line development to the decode circuit via the system bus and transferring the developed liquid ejection data to the system bus (Col 27 Lines 62 – 64).

As per claim 12, Lapstun teaches wherein the compressed liquid ejection data is run length compression data, and the decode circuit can perform hardware development on run length compression data (Figure 19 Items 157 and 158, Col 28 Lines 51 – 53).

As per claim 13, Lapstun teaches a liquid ejecting apparatus comprising the apparatus as claimed in claims 1 and 12 (Figure 2 – 8, Col 4 Lines 25 – 35).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 4 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lapstun et al. US Patent No. 6,687,022 (hereinafter Lapstun) in view of Applicants Admitted Prior Art (hereinafter AAPA).

As per claim 4, Lapstun teaches a data transferring apparatus for transferring liquid ejection data, comprising: a system bus (Lapstun; Figure 17 Item 145); an interface unit for receiving liquid ejection controlling data which comprises liquid ejection data compressed to be capable of line development (Lapstun; Figure 17, Col 26 Lines 21 – 23); a receiving buffer unit comprising an interface memory for storing liquid ejection data compressed to be capable of line development (Lapstun; Figure 18 Item 146, Col 26 Lines 23 – 24); a decode unit comprising a decode circuit, which can perform hardware development on liquid ejection data compressed to be capable of line development and stored in the interface memory (Lapstun; Figure 17 Item 140; Col 28 Line 19 – Col 33 Line 41); a system memory for storing the liquid ejection data developed in the decode circuit (Lapstun; Figure 17 Item 82); a head controlling unit (Lapstun; Figure 17 Item 63); and wherein the interface unit, receiving buffer unit, the decode unit, and the system memory are coupled to the system bus in order to be able to transfer data (Lapstun; Figure 17).

Lapstun does not teach wherein the head controlling unit comprising a register of a liquid ejecting head.

AAPA teaches wherein the head controlling unit comprises a register of a liquid ejecting head (AAPA; Figure 15 Item 13, Page 2 Paragraph [0006]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Lapstun to include the register in the head controlling unit because this allows for the printhead to use data from the register and record an image (AAPA; Page 2 Paragraph [0006]).

As per claim 11, Lapstun in view of AAPA does not teach wherein one (1) Application Specific Integrated Circuit (ASIC) comprises the interface unit, the receiving buffer unit, the decode unit, and the head controlling unit.

Official Notice is taken that use of ASIC circuitry is notoriously well known in the art as it provides a design with a specific application in mind and thus it is optimized for that application from the viewpoint of performance.

9. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lapstun et al. US Patent No. 6,687,022 (hereinafter Lapstun) in view of Applicants Admitted Prior Art (hereinafter AAPA) as applied to claims 4 and 11 above and further in view of FreeBSD Developers' Handbook Chapter 9 DMA (hereinafter FreeBSD).

As per claim 2, Lapstun teaches a data transferring apparatus for transferring liquid ejection data including decode unit comprising a line buffer for storing the liquid ejection data developed by the decode circuit by word unit (Lapstun; Figures 29 and 30, Col 37 Lines 9 – 25).

Lapstun does not teach a DMA transferring unit for performing DMA transfers on the liquid ejection data compressed to be capable of line development to the decode

circuit from the system memory, performing DMA transfers on the liquid ejection data developed in the line buffer to the system memory by word unit, and performing sequential DMA transfer on the developed liquid ejection data stored in the system memory to a register of a liquid ejecting head.

AAPA teaches a transferring unit for performing transfers on the liquid ejection data compressed to be capable of line development to the decode circuit from the system memory (AAPA; Figure 15 Item A, Page 2 Paragraph [0006]), performing transfers on the liquid ejection data developed in the decode circuit to the system memory (AAPA; Figure 15 Item B, Page 2 Paragraph [0006]), and performing sequential transfers on the developed liquid ejection data stored in the system memory to a register of a liquid ejecting head (AAPA; Figure 15 Item C, Page 2 Paragraph [0006]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Lapstun to include the data transfers because they allow for speeding up the data transfer process as suggested by Applicant (AAPA; Pages 2 and 3 Paragraph [0007]).

Lapstun in view of AAPA does not teach wherein the transfers are DMA transfers.

FreeBSD teaches FreeBSD teaches DMA transferring data from one area of the computer to another (FreeBSD; Chapter 9.1 DMA: What it is and How it Works, Paragraph 1).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of the combination of Lapstun and AAPA to include the DMA transfer because DMA transfers allow movement of data from one location to another without intervention from a central processing unit (CPU) (FreeBSD; Chapter 9.1 DMA: What it is and How it Works, Paragraph 1).

As per claim 3, Lapstun and AAPA also teaches wherein the line buffer further comprises two (2) faces of buffer areas for storing developed data and the liquid ejection data developed by the decode circuit is sequentially stored in the first face of the buffer, while the liquid ejection data developed by the decode circuit is sequentially stored in a second face of the buffer areas (Lapstun; Figures 29 and 30, Col 37 Lines 9 – 25); and transfers to the system memory is performed (AAPA; Figure 15 Item B, Page 2 Paragraph [0006]).

10. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lapstun et al. US Patent No. 6,687,022 (hereinafter Lapstun) in view of Applicants Admitted Prior Art (hereinafter AAPA) further in view of FreeBSD Developers' Handbook Chapter 9 DMA (hereinafter FreeBSD) as applied to claims 2 and 3 above and further in view of Chiba et al. US Patent No. 6,665,088 (hereinafter Chiba).

As per claim 5, Lapstun teaches wherein the decode unit comprises a line buffer for storing the liquid ejection data developed by the decode circuit be word unit (Lapstun; Figures 29 and 30, Col 37 Lines 9 – 25).

Lapstun does not teach a DMA transferring unit for performing DMA transfers on the liquid ejection data compressed to be capable of line development to the decode circuit from the interface memory, performing DMA transfers on the liquid ejection data developed in the line buffer to the system memory by word unit.

AAPA teaches performing transfers on the liquid ejection data developed in the decode circuit to the system memory (AAPA; Figure 15 Item B, Paragraph [0006]); and performing transfers on the liquid ejection data from the system memory to a register of a liquid ejecting head (AAPA; Figure 15 Item C, Paragraph [0006]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Lapstun to include the transfer from system memory to the liquid ejecting head because it allows for speeding up the data transfer process as suggested by Applicant (AAPA; Pages 2 and 3 Paragraph [0007]).

Lapstun in view of AAPA does not teach wherein the transfers are DMA transfers.

FreeBSD teaches DMA transferring data from one area of the computer to another (FreeBSD; Chapter 9.1 DMA: What it is and How it Works, Paragraph 1).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of the combination of

Lapstun and AAPA to include the DMA transfer because DMA transfers allow movement of data from one location to another without intervention from a central processing unit (CPU) (FreeBSD; Chapter 9.1 DMA: What it is and How it Works, Paragraph 1).

Lapstun in view of AAPA in view of FreeBSD does not teach performing DMA transfers on the liquid ejection data compressed to be capable of line development to the decode circuit from the interface memory.

Chiba teaches performing DMA transfers on the liquid ejection data compressed to be capable of line development to the decode circuit (Chiba; Figure 1 Item 15) from the interface memory (Chiba; Figure 1 Item 21, Col 5 Lines 59 – 67).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of the combination of Lapstun, AAPA, and FreeBSD to include the transfer of Chiba in order to relieve the processor of the time consuming data transfer.

As per claim 6, Lapstun, AAPA, and FreeBSD further teach wherein the line buffer further comprises two (2) faces of buffer areas for storing developed data and the liquid ejection data developed by the decode circuit is sequentially stored in the first face of the buffer, while the liquid ejection data developed by the decode circuit is sequentially stored in a second face of the buffer areas (Lapstun; Figures 29 and 30, Col 37 Lines 9 – 25), transferring to system memory (AAPA; Figure 15 Item C,

Paragraph [0006]), and wherein the transfer is a DMA transfer (FreeBSD; Chapter 9.1 DMA: What it is and How it Works, Paragraph 1).

Allowable Subject Matter

11. Claims 7 – 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and upon the submission of a proper Terminal Disclaimer.

12. The following is a statement of reasons for the indication of allowable subject matter:

Claims 7 – 9 are allowable because the prior art of record fails to teach or suggest alone or in combination having a first dedicated bus for coupling the interface unit to the receiving buffer unit; a second dedicated bus for coupling the receiving buffer unit to the decode unit; and a third dedicated bus for coupling the decide unit to the head controlling unit and wherein the receiving buffer unit or interface unit comprises a command storing register which is accessible from the system bus, a header analyzing unit for analyzing a header of the liquid ejection controlling data, a command separating unit for separating a command from the liquid ejection controlling data according to the analysis result of the header analyzing unit and storing the command into the command storing register, and a data transfer controlling unit for storing liquid ejection controlling data, from which the command is separated, into the interface memory in combination with the other claimed elements.

Claim 10 is allowable because prior art of record fails to teach or suggest alone or in combination having a first dedicated bus for coupling the interface unit to the receiving buffer unit; a second dedicated bus for coupling the receiving buffer unit to the decode unit; and a third dedicated bus for coupling the decide unit to the head controlling unit and wherein the receiving buffer unit further comprises a data transfer controlling unit for storing liquid ejection controlling data received by the interface unit, and a data separating unit for separating said liquid ejection controlling data stored in said interface memory into a command and liquid ejection data compressed to be capable of line development, wherein said command is processed by a microprocessor coupled to said system bus, and said liquid ejection data compressed to be capable of line development is transferred to said decode unit in combination with the other claimed elements.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard Franklin whose telephone number is (571) 272-0669. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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KIM HUYNH
SUPERVISORY PATENT EXAMINER
2/16/06